REMARKS

This response is intended as a complete response to the Office Action dated August 8, 2005. In view of the following discussion, the Applicants believe that all claims are in allowable form.

CLAIM REJECTIONS

Claims 1-17 and 40-45 stand rejected as being unpatentable over United States Patent No. 6,797,633, issued September 28, 2004, to *Jiang, et al.* (hereinafter *Jiang*) in view of United States Patent Application Publication Serial No. 2004/0161930, published August 19, 2004 to *Ma, et al.* (hereinafter *Ma*), United States Patent No. 6,797,633, issued July 30, 2002 to *Ikeda* (hereinafter *Ikeda*), Taiwan Patent 544,815 published August 1, 2003 to *Chun, et al.* (hereinafter *Chun*), and United States Patent 6,177,147 issued on January 23, 2001 to *Samukawa, et al.* (hereinafter *Samukawa*). The Applicants respectfully disagree.

Independent claims 1 and 40 recite limitations not taught or suggested by any combination of the cited references. *Jiang* describes a method for forming a dual damascene trench patterning method. However, *Jiang* fails to teach or suggest etching in-situ the cap layer, a trench in the second dielectric layer, the masking material, and the second barrier layer, by providing a plasma source power of at least about 1,000 Watts and a bias power of at least about 800 Watts, as recited in claims 1 and 40.

Ma discloses a method of *in-situ* discharge prior to a plasma etch in order to avoid arcing within the chamber during the plasma etch process. (*Ma*, paragraph [0001].) *Ma* further discloses applying an RF power in the range of 100 to 1000 Watts for a 200 mm wafer and from 100 to 2000 Watts for a 300 mm wafer. (*Ma*, paragraph [0028].) However, *Ma* is silent regarding the bias power applied. As such, *Ma* fails to teach or suggest a modification of *Jiang*, alone or in combination with any of the other cited references, that would yield a plasma source power of at least 1,000 Watts and a bias power of at least about 800 Watts during at least a portion of the etch step, as recited in claims 1 and 40.

Moreover, although the Examiner contends that it would have been obvious to modify the etch steps of *Jiang* using the power, pressure, and flow rates as taught by the discharge sequence of *Ma* in order to avoid arcing during the plasma etch processes, *Ma* discloses that the discharge sequence is performed prior to the plasma etch process. (*Ma*, paragraph [0014]). Specifically, *Ma* states that no etching of the photoresist layer or substrate occurs during the discharge sequence. (*Ma*, paragraph [0028]). As such, *Ma* teaches away from the combination being suggested by the Examiner. Instead, the combination of *Ma* and *Jiang* would result in a method wherein a discharge step that does not etch the substrate would be performed prior to plasma etching in order to avoid arcing. Thus, there is no suggestion to modify the etch steps of *Jiang* with the process conditions of the discharge sequence taught by *Ma*, in a manner that would yield the limitations recited in claims 1 and 40.

Ikeda discloses a method of manufacturing a semiconductor device wherein multiple etch steps are provided for etching different layers formed on a substrate. One step of the etch process provides 1600W of electricity to an upper electrode and 1400W of electricity to a lower electrode. The Examiner asserts that it would have been obvious to modify *Jiang* with the power, pressure, and flow rates as taught by *Ikeda* to "reduce the F radicals which form a hardened surface layer." (Office Action, p. 6, ll. 3-11.) The Applicants respectfully disagree.

Ikeda provides no suggestion or motivation to modify the etch process as taught by *Jiang* (alone or modified by any of the cited references) in a manner that yields the limitations recited in claims 1 and 40 because *Ikeda* teaches a different mechanism to reduce F radicals in the process chamber. Specifically, *Ikeda* teaches that, in a parallel plate plasma etcher, "to reduce the excessively generated F radicals, the upper electrode 703 is made of Si, which has high reactivity for F radicals. That is, the excessively generated F radicals are trapped by Si of the upper electrode so that F radicals are reduced." (*Ikeda*, col. 2, ll. 40-44.)

In addition, *Ikeda* teaches that sputtered Si from the upper electrode may deposit on the photoresist and form a hardened resist surface layer. *Ikeda* further teaches that the electricity to the upper electrode should be removed – *i.e.*, the upper electrode should be grounded – to cause a reduction in excess Si atoms which prevents the hardened surface layer from being formed on the photoresist. (*Id.*, col. 5, ll. 61-67.) Therefore, if one wished to prevent the hardened surface layer from being formed on the photoresist, the upper electrode should be grounded.

As such, the motivation provided by the Examiner to combine *Ikeda* and *Jiang* would result in a process that is modified by either or both of forming an upper electrode of silicon and/or connecting the upper electrode to ground. As such, the combination of *Ikeda* and *Jiang* (alone or modified by any of the cited references) fails to yield a plasma source power of at least about 1,000 W and a bias power of at least about 800 W during at least a portion of the etch step, as recited in claims 1 and 40.

Chun discloses a process for etching a nitride layer and an oxide layer using O_2, N_2, and CF_4 in a ratio of O_2:N_2:CF_4 equal to 4-50:0-10:1. *Chun* further discloses applying an RF power in the range of 100 to 1000 Watts but is silent regarding any bias power applied. (*Chun*, Abstract.) As such, *Chun* fails to teach or suggest a modification of any combination of *Jiang*, *Ma*, and *Ikeda* that would yield a plasma source power of at least about 1,000 W and a bias power of at least about 800 W during at least a portion of the etch step, as recited in claims 1 and 40.

Samukawa discloses a process and apparatus for treating a substrate using an ultra-high frequency (UHF) plasma. *Samukawa* further generally discloses applying a UHF RF power in the range of 0 to 1000 Watts but is silent regarding the bias power applied. (*Samukawa*, Figs 3, 6-8, and accompanying text.) As such, *Samukawa* fails to teach or suggest a modification of any combination of *Jiang*, *Ma*, *Ikeda*, and *Chun* that would yield a plasma source power of at least about 1,000 Watts and a bias power of at least about 800 Watts during at least a portion of the etch step, as recited in claims 1 and 40.

As such, a *prima facie* case of obviousness has not been established because the combination of the cited references fails to yield all of the limitations recited in each of independent claims 1 and 40, and claims 2-17 and 41-45, respectively depending therefrom. Specifically, the combination of the cited references fail to teach or suggest a plasma source power of at least about 1,000 Watts and a bias power of at least about 800 Watts during at least a portion of the etch step, as recited in claims 1 and 40.

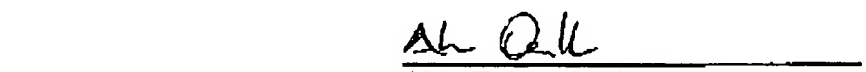
Thus, independent claims 1 and 40, and claims 2-17 and 41-45, respectively depending therefrom, are patentable over *Jiang* in view of *Ma, Ikeda, Chun,* and *Samukawa*. Accordingly, the Applicants respectfully request that the rejection be withdrawn and the claims allowed.

CONCLUSION

Thus, the Applicants submit that all claims now pending are in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issuance are earnestly solicited.

If, however, the Examiner believes that any unresolved issues still exist, it is requested that the Examiner telephone Mr. Alan Taboada at (732) 935-7100 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,



Alan Taboada, Attorney
Reg. No. 51,359
(732) 935-7100

Moser IP Law Group
1040 Broad Street, 2nd Floor
Shrewsbury, NJ 07702